

**AMENDMENTS TO THE SPECIFICATION:**

**On page 1, please insert the following after the title:**

This application is a divisional of prior application Serial No. 09/920,927, filed on August 3, 2001, which is a divisional of prior application Serial No. 08/876,908, filed June 16, 1997, now U.S. Patent No. 6,344,692.

**Please replace the paragraph beginning at page 19, line 22, with the following re-written paragraph:**

Next, with reference to Figs. 3A to 13, a method of forming contact windows of DRAM by self align contact (SAC) techniques will be specifically described. Figs. 3A to 13 are schematic cross sectional views showing a memory cell area taken along line A-A['] of Fig. 2 and a typical wiring structure of a peripheral circuit area. It may be noted that line A-A['] crosses both the word line 12 and the bit line 13.

**Please replace the paragraph beginning at page 20, line 13, with the following re-written paragraph:**

The p-channel MOS transistor area may be an n-type well formed in a p-type silicon substrate, and the n-channel MOS transistor area may be a p-type well formed in the p-type silicon substrate or a p-type well (triple-well structure) formed in an n-type well in the p-type silicon substrate. These structures may be selected as desired according to the design characteristics. For example, reference may be made to US patent application, Serial Number 08/507,978, filed on July 27, 1995, now U.S. Patent No. 5,780,907, claiming priority of September 22, 1994, which is incorporated herein by reference.

**Please replace the paragraph beginning at page 61, line 1, with the following re-written paragraph:**

**CLAIMS We Claim:**